Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **A1**
2. **B1**
3. **Y1**
4. **A2**
5. **B2**
6. **Y2**
7. **GND**
8. **Y3**
9. **A3**
10. **B3**
11. **Y4**
12. **A4**
13. **B4**
14. **VCC**

**.036”**

**.046”**

**9**

**10**

**11**

**12**

**5**

**4**

**3**

**2**

**13 14 1**

**8 6**

**7**

**MASK**

**REF**

**L003Z**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: L003Z**

**APPROVED BY: DK DIE SIZE .036” X .046” DATE: 2/6/18**

**MFG: FAIRCHILD THICKNESS .010” P/N: 54LS03**

**DG 10.1.2**

#### Rev B, 7/1